ABSTRACT OF THE DISCLOSURE

A semiconductor technique is provided which can achieve both of lowered resistance in a logic formation region and reduced leakage current of the capacitor of a memory device. Source/drain regions (4) are formed in the upper surface of a semiconductor substrate (1) in a memory formation region and cobalt silicide films (9) are formed in the upper surfaces of the source/drain regions (4). Source/drain regions (54) are formed in the upper surface of the semiconductor substrate (1) in a logic formation region and cobalt silicide films (59) are formed in the upper surfaces of the source/drain regions (54). The cobalt silicide films (59) in the logic formation region are thicker than the cobalt silicide films (9) in the memory formation region.